ZeusCORE™ MSS IP

1 – 112Gbps DSP Super Long Reach Multi-Standard

About AlphaWave

AlphaWave IP is a leading provider of DSP based silicon IP and chiplet solutions targeted for **Data Processing** (Datacenter/Compute) and **Data Generation** (Optic/Retimer) and **Data Storage** (SSD/Flash)

Management Team

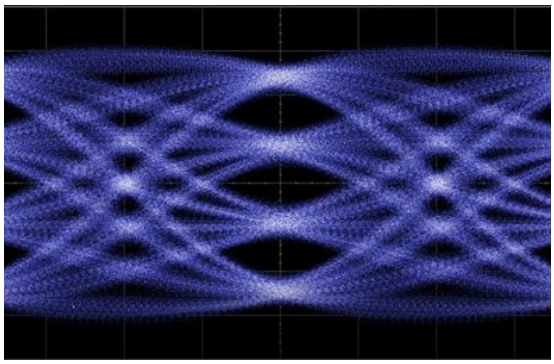
Founded by a team of leading technologists and Silicon Valley entrepreneurs, all with a history of building successful silicon IP businesses and technologies to drive next generation connectivity

Execution Status

- **2018:** First AlphaCORE™ TSMC N7 Silicon is back
- **2019:** AlphaCORE™ N7 IP in production and AlphaCORE™ ported to TSMC N5
- **2020:** Taped out production version of AlphaCORE™ in N6 and N5

ZeusCORE™ IP Highlights

- Super long reach Serdes IP, register configurable architecture operates continuously from 1.0625Gbps to 112Gbps
- Maximum Likelihood Sequence Detector (MLSD) provides up to 3dB of perfomance boost
- Support 40+dB bump-bump at 112G PAM4 with less than 7mW/Gbps for 1 lane of data



Overview

The Alphawave ZeusCORE™ PHY IP is a Super long reach, low-power, Multi-Standard SerDes (MSS) IP. It is a highly configurable IP for all leading edge data center standards from 1Gbps to 112Gbps, optimized for 40+dB bump-bump lossy channel. What differentiates ZeusCORE is the addition of a Most Likely Sequence Detector (MLSD) that significantly extends the channel reach performance.

Configurability

The brilliance of the Alphawave ZeusCORE™ PHY IP is in its patented, register configurable DSP architecture. The ZeusCORE™ Most Likely Sequence Detector (MLSD) uses Viterbi Detection to make slicing decisions based on a sequence of data symbols. Minimizes error across a sequence of symbols and improves Signal-Noise Ratio

AlphaWave IP

Connecting the Digital World

ZeusCORE™ MSS IP
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Power Consumption

Ultra-low-power, DSP based architecture consumes less than 7mW/Gbps for 112G PAM4 Ethernet standards

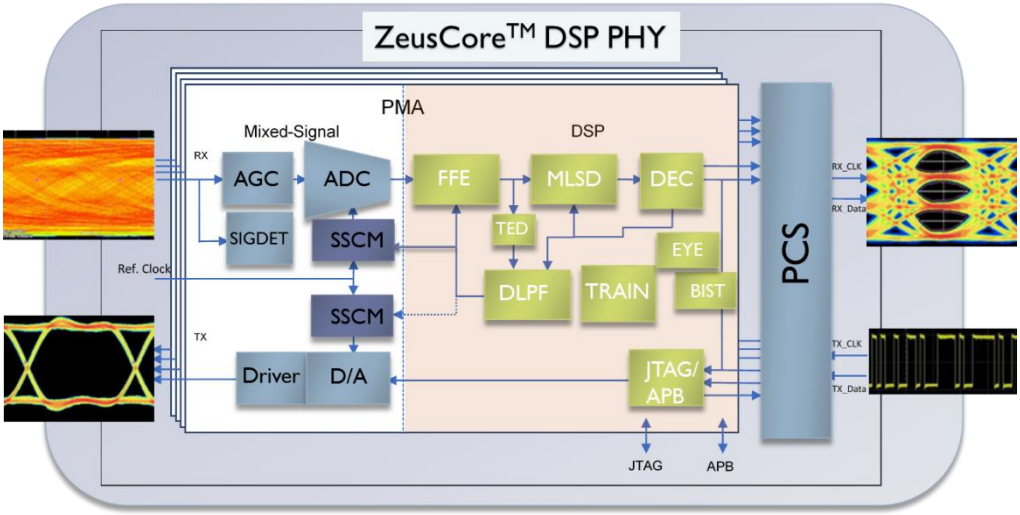
Area Consumption

The ZeusCORE™ DSP MSS IP delivers world leading 473Gbps of IO bandwidth density per millimeter of silicon IO. The ZeusCORE™ IP is available in 1/2/4/8 or 16 lane configurations, as well as both N/S and E/W orientations

Target Channels

Innovative ADC and DSP architecture supports super long reach channel losses greater then 40db PAM4 with with NEXT. The ZeusCORE™ MSS also supports short-reach, high bandwidth interfaces to fiber interconnects. ZeusCORE™ power can be optimized for both shorter channels and lower data rates

ZeusCORE™ Features



- The ZeusCORE™ MSS IP employs a high speed A/D architecture that has configurability for both the A/D sampling rate as well as the A/D resolution
- The ZeusCORE™ CDR employs a wide tuning, sub-sampling clock multiplier that can track over 5000ppm error for both scrambled and 8B/10B encoded data
- The ZeusCORE™ DSP Master Controller includes:
  - All required training is integrated, without the need of external RAM
  - Non-destructive eye monitoring
  - 1+D Partial Response Coding
- Maximum Likehood Sequence Detector (MLSD) provides up to 3dB boost and it can be disabled for shorter channels

Key Specifications

Parameter	Design Specification
Receive Equalization	Designed for closed eye, backplane systems greated then 40db of insertion loss at Nyquist for PAM4 with high MLSD. Includes blind adaptive equalizer and channel estimator
Output Driver Voltage	Programmable 400 – 1200 mVdiff-pkpk (inner eye)
Supply Voltages	Core - 0.75V IO - 1.2V
Devices Used	Core – SVT, LVT and ULVT IO - 1.8V SVT

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