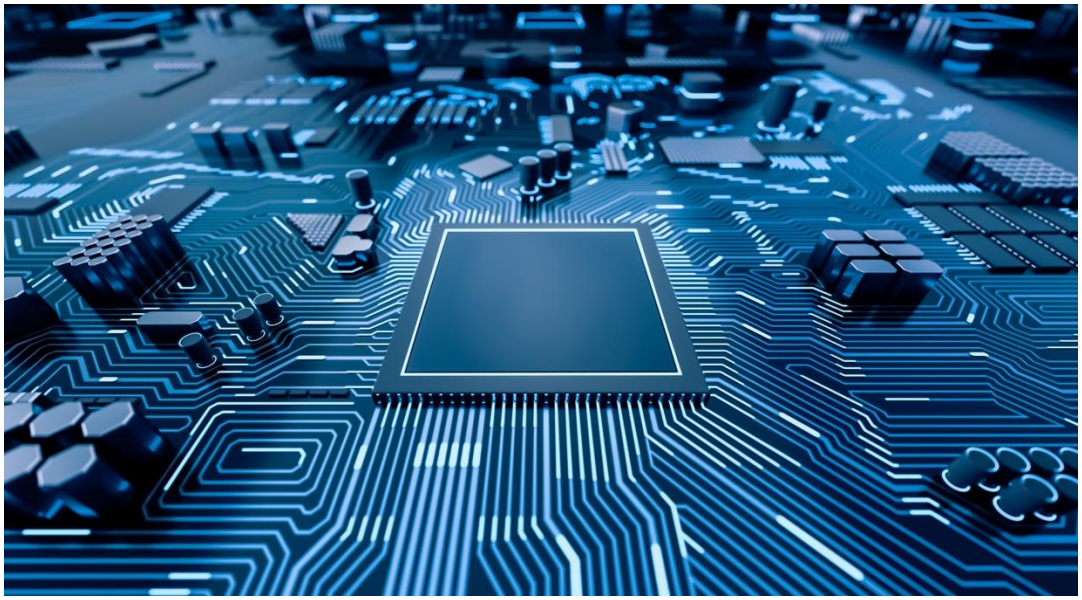
PipeCORE™ PCI-Express (PCIe) PHY

1 – 64Gbps, PCI-Express Gen1-Gen6 PHY



About AlphaWave

AlphaWave IP is a leading provider of DSP based silicon IP and chiplet solutions targeted for **Data Processing** (Datacenter/Compute) and **Data Generation** (Optic/Retimer) and **Data Storage** (SSD/Flash)

Management Team

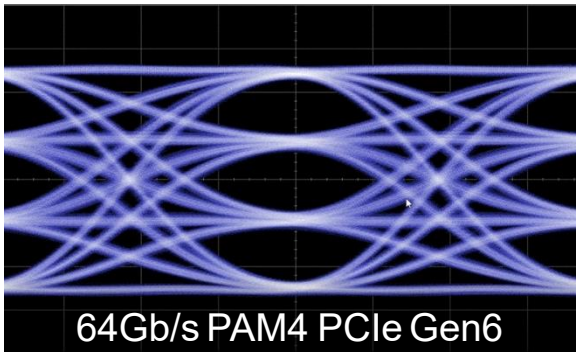
Founded by a team of leading technologists and Silicon Valley entrepreneurs, all with a history of building successful silicon IP businesses and technologies to drive next generation connectivity

Execution Status

- **2018:** First AlphaCORE™ TSMC N7 Silicon is back
- **2019:** AlphaCORE™ N7 IP in production and AlphaCORE™ ported to TSMC N5
- **2020:** Taped out production version of AlphaCORE™ in N6 and N5

PipeCORE™ IP Highlights

- Low power, DSP based architecture provides robust operation over long copper backplanes
- Integrated microcontroller per lane enables fast PCI-Express (PCIe) training in both foreground and background.
- Low power DSP architectures consumes less than 280mW for 1 lane of data operating at 64Gbps



64Gb/s PAM4 PCIe Gen6

Overview

The Alphawave PipeCORE™ PHY IP is a high-performance, low-power, PCI-Express Gen1 – Gen5 PHY that is capable also operating at 64Gbps PAM4 Gen6 rates. It includes a hardened PMA layer and a soft PCS layer deliverable. The PipeCORE™ is based on the industry leading AlphaCORE DSP architecture. The PipeCORE™ is power and performance optimized for the strenous challenges of PCI-Express.

Configurability

The brilliance of the Alphawave PipeCORE™ DSP PHY IP is in its patented, register configurable DSP architecture. The PipeCORE™ leverages high performance A/D converters to digitize incoming data over copper or fiber. The PipeCORE™ DSP Master Controller uses patented signal processing techniques to properly equalize the PCIe channel during link training.

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Power Consumption

Ultra-low-power, DSP based architecture consumes less than 280mW/Channel for 64G PCI-Express

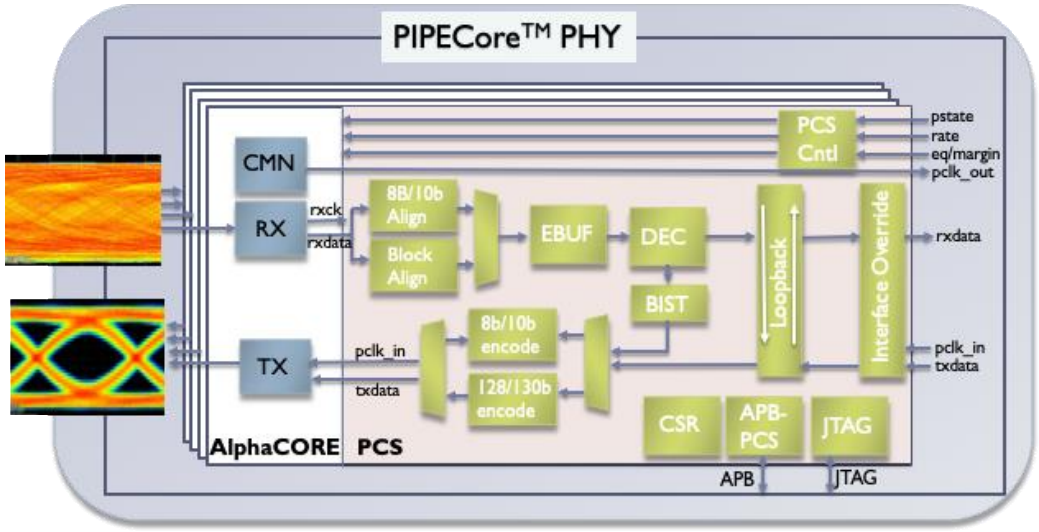
Area Consumption

The PipeCORE PHY delivers world leading 373Gbps of IO bandwidth density per millimeter of silicon IO. The PipeCORE™ IP is available in 1/2/4/8 or 16 lane configurations, as well as both N/S and E/W orientations

Target Channels

Innovative ADC and DSP architecture supports long reach channel losses up to 45dB NRZ with Near-End Crosstalk (NEXT). The PipeCORE™ MSS can also support next generation PCI-Express Gen6 - 64Gbps PAM4 rates. The PipeCORE allows users to safeguard future products with built in upgrade capabiities for next generation PCIe rates.

PipeCORE™ Features



- The PipeCORE™ PHY IP employs a high speed A/D architecture that has configurability for both the A/D sampling rate as well as the A/D resolution
- The PipeCORE™ CDR employs a wide tuning, sub-sampling clock multiplier that can track over 5000ppm error for SRIS applications
- The PipeCORE™ DSP Master Controller includes:
  - All required training is integrated, without the need of external CPU
  - Instantly re-initializes equalizer values after initial training for fast rate changes
- PCIe Gen1-5 PCS layer support both PIPE 4.X and 5.X Message Bus interfaces

Key Specifications

Parameter	Design Specification
Receive Equalization	Designed for closed eye, backplane systems up to 45dB of insertion loss at Nyquist for with NEXT High bandwidth digital CDR meets strict PCIe Jitter Tolerance
Output Driver Voltage	Programmable 400 – 1200 mVdiff-pkpk (inner eye)
Supply Voltages	Core - 0.75V IO - 1.2V
Devices Used	Core – SVT, LVT and ULVT IO - 1.8V SVT

AlphaWave IP
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