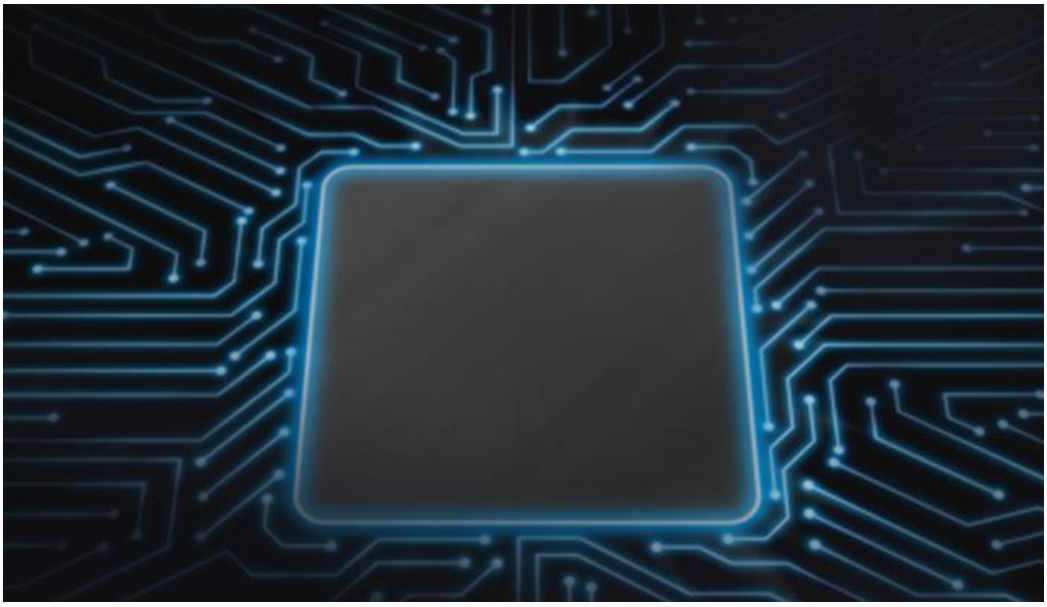
ApolloCORE™ MSS IP

112Gbps MR/VSR Multi-Standard SerDes



About AlphaWave

AlphaWave IP is a leading provider of DSP based silicon IP and chiplet solutions targeted for **Data Processing** (Datacenter/Compute) and **Data Generation** (Optic/Retimer) and **Data Storage** (SSD/Flash)

Management Team

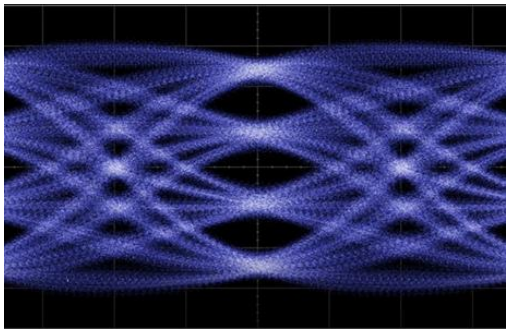
Founded by a team of leading technologists and Silicon Valley entrepreneurs, all with a history of building successful silicon IP businesses and technologies to drive next generation connectivity

Execution Status

- **2018:** First AlphaCORE™ TSMC N7 Silicon is back
- **2019:** AlphaCORE™ N7 IP in production and AlphaCORE™ ported to TSMC N5
- **2020:** Taped out production version of AlphaCORE™ in N6 and N5

ApolloCORE™ IP Highlights

- Low power, register configurable architecture operates continuously from 1.0625Gbps to 112Gbps
- Dynamic architecture can support all modern Data Center standards NRZ and PAM4
- Otimized for Medim Reach (MR) and Very Short Reach (VSR) Application



Overview

The Alphawave ApolloCORE™ MSS IP is a MR/VSR optimized SerDes architecture. What differentiates AppolloCORE in the AlphawaveIP portfolio is the power and area savings for applications that support for MR and shorter channels.
It is high configurable IP and supports all leading edge NRZ and PAM data center standard from 1Gbps to 112Gbps

Power Optimization

The Alphawave ApolloCORE™ delivers delivers a power-optimized less then 3.5mW/Gbps IP solution with up to 373 Gbps of data throughput per millimeter of silicon perimeter. The MR/VSR Architecture deliveres 40% power savings comparing to leading long reach SerDes while, still providing robust equalization for MR and VSR channels

AlphaWave IP
Connecting the Digital World

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Power Consumption

Power optimized, mediun reach and very short reach architecture consumes less than 3.5mW/Gbps for 112G PAM4 data center standards

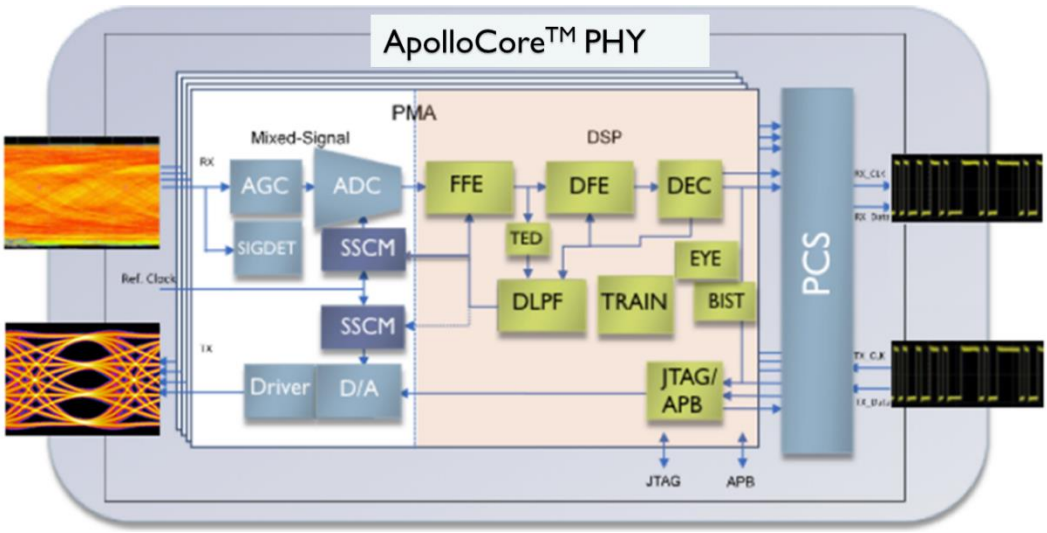
Area Consumption

The ApolloCORE™ MSS IP delivers world leading 373Gbps of IO bandwidth density per millimeter of silicon IO. The ApolloCORE™ IP is available in 1/2/4/8 or 16 lane configurations, as well as both N/S and E/W orientations

Target Channels

Innovative low power architecture supports Very Short Reach (VSR) channel losses up to 15dB. The ApolloCORE™ MSS also supports Medium Reach (MR), high bandwidth interfaces up to 24dB of loss

ApolloCORE™ Features



- The ApolloCORE™ MSS IP employs a high speed analog front end that has configurability to support both PAM4 and NRZ signalling
- The ApolloCORE™ CDR employs a wide tuning, sub-sampling clock multiplier that can track hundreds of ppm frequency error and provide continuous tracking
- The ApolloCORE™ Master Controller includes power sequencing to alleviate the need of an external CPU
- The ApolloCORE™ also supports VSR compatible Ethernet links for short reach communications using 10G, 25G, 56G or 112G Ethernet protocol

Key Specifications

Parameter	Design Specification
Receive Equalization	Designed for MR/VSR based systems up to 15dB of insertion loss at Nyquist for PAM4 Includes blind adaptive receive equalizer
Output Driver Voltage	Programmable 200 – 750 mVdiff-pkpk
Supply Voltages	Core - 0.75V IO - 1.2 V
Devices Used	Core – SVT, LVT and ULVT IO - 1.8V SVT

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